

What is claimed is:

Sub 1

1. A semiconductor integrated circuit, comprising:
a ROM having bit lines extending in a first direction in a first layer; and

a conductive line arranged in a second layer, located above the first layer, wherein

the conductive line partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines.

2. A semiconductor integrated circuit, according to claim 1, wherein

the conductive line is shaped to be a step form having a part extending in the first direction.

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3. A semiconductor integrated circuit, according to claim 1, wherein

the conductive line is shaped so as to pass across the bit lines as many as possible.

4. A semiconductor integrated circuit, according to claim 1, wherein

the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

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5. A semiconductor integrated circuit, according to claim 1,
wherein

the conductive line has two ends extending toward a right
upper portion and a left lower portion of a ROM block, respectively.

6. A semiconductor integrated circuit, according to claim 1,
wherein

the conductive line has two ends both extending toward the
same side of a ROM block.

7. A semiconductor integrated circuit, comprising:
a ROM having bit lines extending in a first direction in a
first layer; and

a conductive line arranged in a second layer, located above
the first layer, wherein

the conductive line is shaped to be a step form partially
extends in a second direction, which is orthogonal to the first
direction, to pass across the bit lines as many as possible.

8. A smart card, comprising:
a ROM;
a CPU using a runnable program fixed at the time of the
manufacture of the component in the ROM; and

a RAM enables the CPU to enter and use temporary data during its operation, wherein

the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, the conductive line partially extending in a second direction, which is orthogonal to the first direction, to pass across the bit lines.

9. A smart card according to claim 8, wherein the conductive line is shaped to be a step form having a part extending in the first direction.

10. A smart card according to claim 8, wherein the conductive line is shaped so as to pass across the bit lines as many as possible.

11. A smart card according to claim 8, wherein the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

12. A smart card according to claim 8, wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

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13. A smart card according to claim 8, wherein the conductive line has two ends both extending toward the same side of a ROM block.

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14. A smart card, comprising:
a ROM;
a CPU using a runnable program fixed at the time of the manufacture of the component in the ROM; and
a RAM enables the CPU to enter and use temporary data during its operation, wherein
the ROM has bit lines extending in a first direction in a first layer; and a conductive line arranged in a second layer, located above the first layer, wherein the conductive line is shaped to be a step form partially extends in a second direction, which is orthogonal to the first direction, to pass across the bit lines as many as possible.

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15. A method for designing a semiconductor integrated circuit according to claim 1, comprising the steps of:

providing bit lines for a ROM extending in a first direction in a first layer;

providing a conductive line arrangement in a second layer, located above the first layer, by an automatic design technique; and

rearranging the conductive line by a manual design technique so that the conductive line partially extends in a second

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direction, which is orthogonal to the first direction, to pass across the bit lines.

16. A method according to claim 15, wherein the conductive line is shaped to be a step form having a part extending in the first direction.

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17. A method according to claim 15, wherein the conductive line is shaped so as to pass across the bit lines as many as possible.

18. A method according to claim 15, wherein the conductive line has two ends extending toward upper and lower portions of a ROM block, respectively.

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19. A method according to claim 15, wherein the conductive line has two ends extending toward a right upper portion and a left lower portion of a ROM block, respectively.

20. A method according to claim 15, wherein the conductive line has two ends both extending toward the same side of a ROM block.